2017

(April)

COMPUTER SCIENCE

(Elective/Honours)

(Digital Logic Design and Computer Architecture)

(CS–201T)

Marks : 75

Time : 3 hours

The figures in the margin indicate full marks for the questions

Answer **one** question from each Unit

UNIT—I

1. *(a)* State de Morgan's theorem. Draw the logic diagram of the following Boolean expression $F = AB + A'C$. 1+3=4

(b) Prove the *distributive law*

$$x \cdot (y + z) = (x \cdot y) + (x \cdot z)$$

of Boolean algebra with truth table and the gate diagram. 4

(c) Subtract the following using both r's and $(r-1)$'s complements : 2+2=4

(i) $(20)_{10} - (8000)_{10}$

(ii) $(11010)_2 - (10000)_2$

(d) Convert the following to the given base : 1×3=3

(i) $(306.D)_{16} - (\ )_2$

(ii) $(1110101.110)_2 - (\ )_{10}$

(iii) $(12.0625)_{10} - (\ )_8$

2. (a) With the help of logic gate diagram, explain 2-input X-NOR gate and give its truth table. 2+2=4

(b) Obtain the truth table of the following function : 4

$$F = xy + xy' + y'z$$

(c) Show the steps of subtraction with r's and $(r-1)$'s complement with the help of an example. 2+2=4

(d) Obtain the r's and $(r-1)$'s complement of the following : 1×3=3

(i) $(0000001)_2$

(ii) $(09900)_{10}$

(iii) $(1010101)_2$

UNIT—II

3. (a) What is the canonical form of a Boolean expression? Explain with an example. 3

(b) Draw Karnaugh map and simplify the following Boolean function : 6

$F(A, B, C, D) = \Sigma(1, 3, 7, 8, 9, 10, 11, 12)$

$d(A, B, C, D) = \Sigma(0, 6, 14, 15)$

(c) Convert the following into canonical form : 3+3=6

(i) $(A + B' + C)(A + BD')$

(ii) $AC' + BC + BD'$

4. (a) Convert the following expressions to canonical form : 3+3=6

(i) $F(A, B, C, D) = (C' + D')(A + B)(A' + B + D)$

(ii) $F(w, x, y, z) = x + y$

(b) Express the following expressions as a sum of maxterms : 3+3=6

(i) $F(x, y, z) = (xy + z)(x + yz)$

(ii) $F(x, y, z) = 1$

(c) Explain the difference between Dual and Complement of a Boolean expression with examples. 3

UNIT—III

5. *(a)* The content of a 4-bit shift register *A* is initially 1101 and that of 4-bit shift register *B* is initially 0010. Show the content of each register after each shift. 5

(b) Derive the expressions for the Sum and Carry of a full-adder and draw its logic diagram. 4

(c) Explain the Booth algorithm for multiplying negative binary integers in 2's complement form. 6

6. *(a)* An 8-bit register contains the binary value 10011100. What is the register value after arithmetic shift right? Starting from the initial number 10011100, determine the register value after arithmetic left and state whether there will be an overflow. 3+3=6

(b) Using truth table, derive the Boolean expressions for the Sum and Carry of a half-adder. 4

(c) Discuss the various registers used to store the multiplicand, multiplier and product with respect to hardware for Booth's algorithm. 2+2+1=5

UNIT—IV

7. *(a)* What is an intermediate state of an *R-S* flip-flop? How can you solve it with a *J-K* flip-flop? Explain. 1+5=6

(b) What is a counter? Explain the state diagram, excitation table for a 3-bit counter using *T* flip-flop. 1+3=4

(c) What are the possible formats of an instruction code? 5

8. *(a)* What do you understand by present state and next state of a flip-flop? How can you determine the next state of a *D* flip-flop from its present state? 2+4=6

(b) What are control instructions? Explain its various types. 1+3=4

(c) Describe binary up-down counter with a logic diagram. 5

UNIT—V

9. *(a)* Illustrate source initiated strobe for asynchronous data transfer with a labeled diagram. 5

(b) Explain the role of DMA controller during DMA transfer with block diagram. 5

(c) Explain any two mapping techniques used in organization of a cache memory. 2½+2½=5

10. (a) Explain destination initiated data transfer using handshaking with sequence of events diagram. 5

(b) What do you mean by hit and miss ratio in a cache? 2½+2½=5

(c) What is priority interrupt? How can you establish the priority of simultaneous interrupts? 2+3=5

(Internals—25)

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